What is claimed is:

1. Method for function testing an emulated logic circuit wherein a model of a logic circuit is loaded into a hardware emulator (EM) in a hardware description language, wherein:

- the emulated logic circuit is put into an operating mode in which some or all of the flip-flops it contains, in particular with additional logic elements as interfacing circuitry, are functionally chained into one or more shift registers, and
- the structural arrangement of the logic circuit in the hardware emulator (EM) is compared with the structural arrangement of the model of the logic circuit at least partially with the assistance of this operating mode.

2. Method according to Claim 1, wherein:

- a test pattern is applied to inputs (Ix) of the emulator (EM), which simultaneously represent inputs of shift registers, and is shifted into the shift registers by means of suitable pulsing,
- the emulated logic circuit is set to a standard operating mode, one or more pulsing cycles ensue, and the circuit then re-set to the original operating mode,
- the ensuing result pattern is shifted by means of suitable pulsing to emulator (EM) outputs (Ox) which simultaneously represent outputs of the shift registers, and a check is carried out there to determine whether the pattern matches an expected value, and
- this result is used to compare the structural arrangement of the logic circuit in the hardware emulator (EM) with the structural arrangement of the model of the logic circuit.

3. Method according to Claim 1, wherein:

- a test pattern is applied to an emulator (EM) input (Ix) which simultaneously represents the input of a shift register,

- the test pattern is shifted through the shift register by means of suitable pulsing,
- an emulator (EM) output (Ox) which simultaneously represents the output of this shift register is checked for the appearance of this or of the inverted test pattern,
- the number of flip-flops in the shift register is determined from the number of pulsing sequences required for shifting through, and
- this result is used to compare the structural arrangement of the logic circuit in the hardware emulator (EM) with the structural arrangement of the model of the logic circuit.

4. Method according to Claim 3, wherein the output of a shift register (Ox) is connected to the input of a next adjacent shift register (Ix+1) and all shift registers are chained into a single shift register by means of recursion.

5. Method according to one of Claim 1, wherein
- in the event that the structural arrangement of the logic circuit in the hardware emulator (EM) does not match the structural arrangement of the model, an analysis is carried out to determine the sources of such faults, and
- the model of the logic circuit is automatically re-loaded into the hardware emulator (EM) with these sources of faults deactivated.

6. A Device for testing an emulated logic circuit, comprising: a hardware emulator (EM) for emulating a logic circuit present in the form of a model, a test pattern generator module (PC) for applying a test pattern to an input (Ix) of the hardware emulator (EM), a pulse generator for injecting a pulse into the hardware emulator (EM), and a test pattern checking module (PC) for checking whether a bit pattern being applied to an output (Ox) of the hardware emulator (EM) matches an expected value, the device additionally contains a module for comparing the structural arrangement of the logic circuit in the hardware emulator (EM) with the structural arrangement of the model of the logic circuit at least partially with the assistance of an operating mode of the logic circuit in which some or all of the flip-flops it contains, in

particular with additional logic elements as interfacing circuitry, are functionally chained into one or more shift registers.

7. The device according to claim 6, further comprising a module for determining the number of flip-flops in the shift register from the number of pulse sequences needed to shift a test pattern through the register and/or a module for briefly changing over the logic circuit to a standard operating mode for one pulse cycle or several pulse cycles while a test pattern is being shifted through the register.

8. The device according to claim 6, further comprising a module for chaining all the shift register into a single shift register by means of recursively connecting the output (Ox) of, in each case, one shift register to the input (Ix+1) of, in each case, one next adjacent shift register.

9. The device according to claim 6 further comprising

- a module for analyzing the sources of faults leading to a lack of matching between the structural arrangement of the logic circuit in the hardware emulator (EM) and the structural arrangement of the model, and
- a module for automatically loading the model of the logic circuit into the hardware emulator (EM) with these sources of faults deactivated.